IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	En-Hsing Chen et al.		
Title:	NAND MEMORY ARRAY INCORPORATING MULTIPLE SERIES SELECTION DEVICES AND METHOD FOR OPERATION OF SAME		
Application No.:	10/729,865	Filed:	December 5, 2003
Examiner:	Nguyen, Van Thu T.	Group Art Unit:	2824
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APPEAL BRIEF (37 C.F.R. § 41.37)

This brief is in furtherance of the Notice of Appeal filed on January 4, 2007. The fee required under 37 C.F.R. § 41.20(b)(2) is provided as directed in an electronic submission of this paper or in a transmittal letter accompanying this paper.

REAL PARTY IN INTEREST

The real party in interest in this appeal is SanDisk 3D LLC, the assignee of record, as evidenced by the assignment recorded at Reel/Frame 015186/0548, by the merger document recorded at Reel/Frame 017544/0769, and by the corrected merger document recorded at Reel/Frame 018950/0686.

RELATED APPEALS AND INTERFERENCES

Known prior and pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal include:

None.

STATUS OF CLAIMS

Claims 1-20, 22, 23, and 27-54 are pending. Claims 1, 27 and 28 stand as rejected, and claims 2-20, 22, 23, and 29-54 remain withdrawn from consideration. Rejected claims 1, 27 and 28 are the subject of this appeal.

STATUS OF AMENDMENTS

An amendment under 37 C.F.R. § 116 (the "Rule 116 Amendment") was submitted on November 28, 2006 canceling withdrawn claims 55-60 in order to place the application in better form for appeal. In the advisory action mailed December 13, 2006, no indication was provided as to whether the Rule 116 Amendment was or was not entered for purposes of appeal. Applicant believes that the Rule 116 Amendment was proper and has been or will be entered, and the above-mentioned status of claims reflects such entry of the Rule 116 Amendment.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to an integrated circuit comprising a memory array (for example, array 502 shown in Fig. 16) including memory cells arranged in a plurality of series-connected NAND strings (four such strings shown in Fig. 2, described in ¶0049), said memory cells comprising modifiable conductance switch devices (¶0037: "Each NAND string includes a plurality of SONOS transistors, connected in series, each gated by a respective one of a plurality of word lines"), said NAND strings including at a first end thereof (¶0037: "The NAND string 102 *also* includes a block select device 114 for coupling one end of the NAND string to a global bit line 103" (emphasis added)) a respective plurality of series selection devices of like type (Figs. 9, 10, ¶0070, ¶0072), wherein each NAND string includes a second plurality of series selection devices of like type at a second end thereof (¶0037: "The NAND string 102 ... further includes a second block select device 116 for coupling the other end of the NAND string to a shared bias node ..."). Pairs of NAND strings are arranged so that a first group of control signals couples the respective second end of one string of the pair to a global array line associated with the pair, and couples the respective first end of the other string of the pair to a respective bias node (Figs. 2, 9, 10, ¶0070 ("The field enhanced leakage current, particularly of TFT devices, may be reduced by using multiple series selection devices rather than a single

selection device at one or both ends of a NAND string."), ¶0072, Figs. 17D, 18, ¶0087). Pairs of NAND strings are also arranged so that a second group of control signals couples the respective first end of said one string of the pair to a respective bias node, and couples the respective second end of the other string of the pair to the global array line associated with the pair (Figs. 2, 9, 10, ¶0070, ¶0072, Figs. 17D, 18, ¶0087).

The foregoing concise explanation(s) of the subject matter defined in each of the above-identified claim(s), and the corresponding references to the specification and to the drawing, are exemplary and should not to be taken as limiting of the invention.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Ground I: The rejection of claim 1 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,380,636 (hereinafter "Tatsukawa").

Ground II: The rejection of claims 27-28 under 35 U.S.C. § 103(a) as being unpatentable over Tatsukawa in view of U.S. Patent No. 6,411,548 (hereinafter "Sakui").

ARGUMENT

Ground I: The rejection of claim 1 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,380,636 (hereinafter "Tatsukawa").

Claim 1

The Examiner cites Tatsukawa, in Fig. 8, as disclosing a NAND string memory array, each NAND string "including at a first end thereof a respective plurality of series selection devices of like type, wherein each NAND string includes a second plurality of series selection devices of like type at a second end thereof." Relative to the NAND string shown on the left side of Fig. 8, the Examiner cites transistors DG1 and SGD1 as corresponding to the plurality of series selection devices at the first end of the NAND string, and cites transistors SGS1 and DG2 as corresponding to the plurality of series selection devices at the second end of the NAND string.

Applicant agrees with the Examiner's position regarding transistors DG1 and SGD1, but respectfully takes issue with the position regarding transistors SGS1 and DG2. Applicant submits that only transistor SGS1 corresponds to a selection device at this end of this NAND string because the connection to the source line SL1 is made just "beyond" transistor SGS1, as viewed from the perspective of the NAND string. Specifically, the common node between transistors SGS1 and DG2 is itself the source line SL1. Tatsukawa describes the role of transistor DG2 as being for matching purposes in his description regarding Fig. 1 (even though described in the context of a different memory cell arrangement than Fig. 8), to wit:

> These dummy transistors DG1-DG4 are employed so that sub-bit lines SBL1 and SBL2 may have the same electric characteristics (parasitic resistance and parasitic capacitances) and sub-source lines SSL1 and SSL2 may have the same electric characteristics. Owing to these dummy transistors DG1-DG4, the layout of transistors in memory cell unit MU can be symmetrical with respect to main bit line MBL, so that the layout can be made simple, and an influence by misalignment of a mask in a manufacturing process can be cancelled. By arranging the source line between the source select signal lines, the size of the unit in the column direction can be reduced.

(Tatsukawa, column 7, lines 50-61). The source (or drain) region of this transistor DG2 is also shown in Fig. 5 as impurity region 2-1a. This appears to be an unconnected impurity region, as the array shown in Fig. 6 does not indicate any nodes leaving a respective memory cell unit MU except the two connections to the main bit line MBL, nor any other connections common to adjacent memory units MU. Nonetheless, it is not clear whether Tatsukawa intends to "abut" the impurity region 2-1a with the impurity region 1-1a within a second memory cell unit MU adjacent to ("below" as drawn) the one shown in Fig. 5 (see column 10, lines 25-26, "These diffusion layers all extend in the column direction."), or alternately, whether Tatsukawa intends to provide space between such adjacent impurity regions.

A resolution to this question is unnecessary because, in either case, dummy transistor DG2 *cannot be seen as a select device.* A select device within, and at one end of, a NAND string functions to couple a series connected string of memory cells within the NAND string to some kind of memory array node (e.g., global array line, main bit line, bias node, source line, etc.). Tatsukawa's dummy transistor DG2 does not couple memory cells within the NAND

string (i.e., memory cells MC11, MC12) to the source line SL1, and thus cannot be seen as a select device. Rather, only transistor SGS1 functions to couple the memory cells MC11, MC12 to the source line SL1.

Any extraneous transistor structure formed "beyond" the connection to the memory array node in question cannot be part of the NAND string. In this case, the extraneous dummy transistor DG2 is connected to the same source line SL1, but is not part of the NAND string, does not function to select the NAND string, and cannot be seen as being a select device.

As used in the instant application, this transistor DG2 cannot be seen as one of a *plurality* of series select transistors *at one end* of the NAND string (i.e., "each NAND string including at a first end thereof a plurality of series select devices ..."). Consequently this NAND string does not include a plurality of series selection devices at *both ends* of the NAND string.

The similar situation is present for the NAND string shown on the right side of Fig. 8. Applicant submits that transistor DG4 is not part of the NAND string since it lies beyond the connection to node SL2, and consequently the second NAND string likewise does not include a plurality of series selection devices at both of its ends.

The Examiner disagrees with this logic, arguing instead that dummy transistor D2 is a select device for the NAND string, citing Tatsukawa's Figure 1 and associated text as follows:

> Sub-source line SSL1 is connected to a source line SL1 via source-side block select transistor SGS1 made conductive in response to source-side block select signal SS1. This source line SL1 is connected to a source-side *dummy transistor DG2 made conductive on in response to a drain-side block select signal SG2 [SD2?]*. One conduction node (drain) of dummy transistor DG2 is set to the open state. [Emphasis added]

(Tatsukawa, column 7, lines 29-35, describing FIG. 1). The portion which the Examiner chose to emphasize in this passage actually undercuts the Examiner's argument. The dummy transistor DG2 is made conductive in response to a block select signal SD2. When active, this signal SD2 is actually selecting the *other* sub-bit line SBL2 and coupling it to the major bit line MBL (see description regarding Tatsukawa's Figs. 2A, 2B, 3, and 4), *not* the sub-bit line SBL1 to which the Examiner posits the alleged "select" device DG2 somehow relates. The Examiner's

later statement that the "Dummy transistor DG2 turns on/off in response to drain-side block *select signal* SD2, therefore it is seen as a selection device" totally misunderstands or ignores the issue of *which* sub-source line or sub-bit line is being selected, in addition to the fundamental question that such dummy transistor cannot actually participate in *selecting* any of such lines, since its drain terminal is open! It cannot couple a sub-source line to the source line, nor can it couple a sub-bit line to the major bit line. It simply *cannot select anything* and couple it to the source line.

The Examiner also cites the following text in support of her argument:

> Sub-source line SSL2 is connected to a source line SL2 via source-side block select transistor SGS2 made conductive in response to source-side block select signal SS2. This source line SL2 is connected to a source-side *dummy transistor DG4 receiving a drain-side block select signal SG1 [SD1?] on its gate.* One conduction node (drain) of dummy transistor DG4 is set to the open state. *With no channel resistance of the dummy transistor, a resistance between the sub-source line and the source line can be small.* [Emphasis added]

(Tatsukawa, column 7, lines 41-49, describing FIG. 1). The second portion which the Examiner chose to emphasize in this passage above actually undercuts the Examiner's argument even further, and reinforces Applicant's argument that the dummy transistor DG4 is not a select device. Tatsukawa is trying to point out that the resistance that couples the sub-source line SSL2 to the source line SL2 results *only* from the one select transistor SGS2 (i.e., when conductive). This transistor is the only device that actually couples the sub-source line SSL2 to the source line SL2, and is the only transistor that can properly be viewed as a select device at this end of the NAND string.

Lastly, the Examiner also cites the following text in support of her argument:

> *These dummy transistors DG1-DG4 are employed so that sub-bit lines SBL1 and SBL2 may have the same electric characteristics (parasitic resistance and parasitic capacitances)* and sub-source lines SSL1 and SSL2 may have the same electric characteristics. Owing to these dummy transistors DG1-*DG4*, the layout of transistors in memory cell unit MU can be symmetrical with respect to main bit line MBL, so that the layout can be made simple, and an influence by misalignment of a mask in a manufacturing process can be cancelled. By arranging the source line

> between the source select signal lines, the size of the unit in the column direction can be reduced." [Emphasis added].

(Tatsukawa, column 7, lines 50-61, describing FIG. 1). From these passages, the Examiner advances the position that the "dummy transistor DG2 is *selected* for equalizing the electric characteristics between selected sub-bit line SBL2 and unselected sub-bit line SBL1," and thus concludes that "transistor DG2 is seen as a selection device."

Tatsukawa nowhere states that the dummy transistor DG2 is *selected* for equalizing electric characteristics. What Tatsukawa actually *states* is that the transistors DG1-DG4 are *employed* for such purpose. Applicant has already noted that when DG2 is turned on, the *other* sub-bit line is selected. Moreover, the balancing of capacitance of a great many unselected sub-bit lines and sub-source lines may result much more from the presence of these dummy transistors when they are *turned off*, not when they are turned on (i.e., "selected" as the Examiner advances in her argument). Applicant's position in this regard is bolstered by Tatsukawa's statement above that "an influence by misalignment of a mask in a manufacturing process can be cancelled." Such a result would not follow when transistor DG2 is turned on, for its drain node is stated by Tatsukawa (and shown in his drawing) as being open, and thus its drain capacitance would, in fact, be alignment sensitive, and would contribute a variable capacitance term to the capacitance of the node to which the open drain node is coupled (i.e., the source line SL1) when dummy transistor DG2 is turned on. Rather, the total capacitance of the great number of contacts to the source line SL1 throughout the array may be made alignment insensitive by an equally great number of transistors DG2 that are *turned off*. This maintains a constant diffusion area of the SL1 node, irrespective of polysilicon misalignment relative to the active area.

The Examiner agrees with Applicants' argument, expressed in a prior paper as well as here, that dummy transistor DG2 does not couple memory cells within the NAND string to some kind of memory array node. However, she argues that "the claim language, especially claim 1, merely calls for first and second groups of control signals, *not the selection devices,* to couple a series connected string of memory cell within the NAND string to the global array line and bias node." Such a conclusion reads key limitations entirely out of the claim, for claim 1 also recites:

> ... said NAND strings *including* at a first *end thereof* a respective *plurality* of series selection devices of like type, wherein each NAND string

> *includes* a second *plurality* of series selection devices of like type at a second *end thereof* ... [emphasis added]

These are structural limitations that cannot be properly ignored, but that is precisely what the Examiner's argument does. Applicant submits that Tatsukawa fails to disclose each limitation of claim 1, and that the Examiner has therefore not established a prima facie case for anticipation.

For the at least the foregoing reasons, this honorable Board is respectfully requested to reverse the rejection of this claim.

Ground II: The rejection of claims 27-28 under 35 U.S.C. § 103(a) as being unpatentable over Tatsukawa in view of U.S. Patent No. 6,411,548 (hereinafter "Sakui").

Claims 27 and 28

Applicant submits that Tatsukawa fails to disclose each limitation of claim 1 (from which these claims depend). Sakui was not cited by the Examiner as disclosing limitations that would cure this deficiency. The Examiner has therefore not established a prima facie case for obviousness. These two claims are believed allowable at least for their dependence from allowable claim 1. For the at least this reason, this honorable Board is respectfully requested to reverse the rejection of these claims.

CONCLUSION

For the at least the foregoing reasons, Appellants' presently claimed invention was not anticipated under 35 U.S.C. § 102(b) by the cited prior art, and would not have been obvious to one of ordinary skill in the art under 35 U.S.C. § 103(a) in view of the cited prior art. Accordingly, this honorable Board is respectfully requested to reverse the rejections of claims 1, 27, and 28 and to direct the claims of the present application to be issued.

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Respectfully submitted,

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CLAIMS APPENDIX

1. (Previously presented) An integrated circuit comprising a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices, said NAND strings including at a first end thereof a respective plurality of series selection devices of like type, wherein each NAND string includes a second plurality of series selection devices of like type at a second end thereof, and wherein pairs of NAND strings are arranged so that:

a first group of control signals couples the respective second end of one string of the pair to a global array line associated with the pair, and couples the respective first end of the other string of the pair to a respective bias node; and

a second group of control signals couples the respective first end of said one string of the pair to a respective bias node, and couples the respective second end of the other string of the pair to the global array line associated with the pair.

2. (Withdrawn) The integrated circuit as recited in claim 1 wherein the memory array comprises a two-dimensional memory array having one plane of memory cells formed in a substrate.

3. (Withdrawn) The integrated circuit as recited in claim 1 wherein the memory array comprises a three-dimensional memory array having at least two planes of memory cells formed above a substrate.

4. (Withdrawn) The integrated circuit as recited in claim 3 wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

5. (Withdrawn) The integrated circuit as recited in claim 3 wherein the substrate comprises a polycrystalline substrate.

6. (Withdrawn) The integrated circuit as recited in claim 3 wherein the substrate comprises an insulating substrate.

7. (Withdrawn) The integrated circuit as recited in claim 1 wherein the modifiable conductance switch devices comprise transistors having a depletion mode threshold voltage at least some of the time.

8. (Withdrawn) The integrated circuit as recited in claim 20 wherein the modifiable conductance switch devices comprise transistors having a respective threshold voltage which is modifiable post-manufacture.

9. (Withdrawn) The integrated circuit as recited in claim 8 wherein the modifiable conductance switch devices comprise a floating gate electrode.

10. (Withdrawn) The integrated circuit as recited in claim 8 wherein the modifiable conductance switch devices comprise silicon nanoparticles.

11. (Withdrawn) The integrated circuit as recited in claim 8 wherein the modifiable conductance switch devices comprise a polarizable material.

12. (Withdrawn) The integrated circuit as recited in claim 8 wherein the modifiable conductance switch devices comprise a ferroelectric material.

13. (Withdrawn) The integrated circuit as recited in claim 20 wherein the modifiable conductance switch devices comprise thin film transistor (TFT) devices.

14. (Withdrawn) The integrated circuit as recited in claim 8 wherein the modifiable conductance switch devices comprise transistors having a charge storage dielectric.

15. (Withdrawn) The integrated circuit as recited in claim 14 wherein the charge storage dielectric comprises an oxide-nitride-oxide (ONO) stack.

16. (Withdrawn) The integrated circuit as recited in claim 14 wherein the memory cell transistors have a depletion mode threshold voltage when the charge storage dielectric has a minimum stored negative charge level.

17. (Withdrawn) The integrated circuit as recited in claim 14 wherein the memory cell transistors have a depletion mode threshold voltage when the charge storage dielectric has a minimum stored positive charge level.

18. (Withdrawn) The integrated circuit as recited in claim 14 wherein the memory cell transistors have a first depletion mode threshold voltage corresponding to an erased data state and have a second depletion mode threshold voltage corresponding to a programmed data state.

19. (Withdrawn) The integrated circuit as recited in claim 1 wherein the memory cell switch devices have more than two nominal values of conductance, for storing more than one bit of data per memory cell.

20. (Withdrawn) The integrated circuit as recited in claim 1 wherein the selection devices and memory cell devices forming each NAND string are structurally substantially identical.

21. (Canceled)

22. (Withdrawn) The integrated circuit as recited in claim 1 wherein respective select signals corresponding to at least two respective ones of the first plurality of series selection devices for a selected NAND string are driven to different levels during at least one memory operation.

23. (Withdrawn) The integrated circuit as recited in claim 22 wherein, during a programming operation for a selected NAND string, the respective select signal corresponding to one of the first plurality of series selection devices is driven to ground, and the respective select signal corresponding to another one of the first plurality of series selection devices is driven to a voltage between ground and a programming voltage conveyed on a selected word line.

24-26. (Canceled)

27. (Previously presented) The integrated circuit as recited in claim 1 comprising series selection devices having a charge storage dielectric.

28. (Original) The integrated circuit as recited in claim 27 comprising series selection devices which are maintained by periodic programming biasing to a higher threshold voltage than fabricated.

29. (Withdrawn) The integrated circuit as recited in claim 3 wherein NAND strings on more than one memory level are respectively coupled to global array lines disposed on fewer levels than said more than one memory level.

30. (Withdrawn) The integrated circuit as recited in claim 3 wherein a respective plurality of NAND strings on each of at least two memory levels are coupled to a single global array line disposed on a single level of the integrated circuit.

31. (Withdrawn) The integrated circuit as recited in claim 3 wherein the modifiable conductance switch devices comprise thin film transistor (TFT) devices having a charge storage dielectric.

32. (Withdrawn) The integrated circuit as recited in claim 31 wherein the memory cell transistors have a depletion mode threshold voltage when the charge storage dielectric has a minimum stored negative charge level.

33. (Withdrawn) The integrated circuit as recited in claim 31 wherein:
the series selection devices and memory cell devices forming each NAND string are structurally substantially identical.

34. (Withdrawn) The integrated circuit as recited in claim 33 wherein, during a programming operation, a respective select signal corresponding to one of the first plurality of series selection devices is driven to ground, and a respective select signal corresponding to another one of the first plurality of series selection devices is driven to a voltage between ground and a programming voltage conveyed on a selected word line.

35. (Withdrawn) The integrated circuit as recited in claim 34 wherein pairs of NAND strings are arranged so that:

a first group of at least one control signal couples the respective second end of each string of the pair to a respective global array line; and

a second group of control signals couples the respective first end of each string of the pair to a shared bias node.

36. (Withdrawn) The integrated circuit as recited in claim 35 wherein, during a programming operation, the shared bias node is driven to a voltage between ground and a bit line inhibit voltage conveyed to an unselected NAND string sharing word lines with the selected NAND string.

37. (Withdrawn) The integrated circuit as recited in claim 36 wherein, during a programming operation, more than one NAND string is selected in a selected block of the memory array.

38. (Withdrawn) The integrated circuit as recited in claim 1 embodied in computer readable descriptive form suitable for use in design, test or fabrication of said integrated circuit.

39. (Withdrawn) An integrated circuit including a memory array arranged in a plurality of blocks, said integrated circuit comprising:

a first memory block comprising

a first bias node;

a plurality of global bit lines traversing across the first block in a first direction;

a plurality of word lines traversing across the first block in a second direction different than the first direction;

a first group of one or more select lines traversing across the first block generally parallel to and disposed on one side of the plurality of word lines;

a second group of more than one select lines traversing across the first block generally parallel to and disposed on the other side of the plurality of word lines; and

a plurality of series-connected NAND strings, each comprising, at a first end thereof, a first group of one or more series select devices of like type, each responsive to a

respective one of the first group of one or more select lines, further comprising a plurality of memory cell devices each responsive to a respective one of the plurality of word lines, and further comprising, at a second end thereof, a second group of more than one block select devices of like type, each responsive to a respective one of the second group of more than one select lines.

40. (Withdrawn) The integrated circuit as recited in claim 39 wherein:

the first end of each NAND string is respectively coupled to a respective one of the plurality of global bit lines; and

the second end of each NAND string is respectively coupled to the first bias node.

41. (Withdrawn) The integrated circuit of claim 40 comprising global bit lines disposed on more than one global bit line layer.

42. (Withdrawn) The integrated circuit of claim 41 comprising even-numbered global bit lines disposed on a first global bit line layer and odd-numbered global bit lines disposed on a second global bit line layer.

43. (Withdrawn) The integrated circuit of claim 40 wherein global bit lines respectively associated with each of a pair of adjacent NAND strings are disposed on different layers of the integrated circuit.

44. (Withdrawn) The integrated circuit as recited in claim 39:

wherein the first memory block further comprises a second bias node;

wherein the first end of each of a first group of the NAND strings is respectively coupled to a corresponding one of the plurality of global bit lines, and the first end of each of a second group of the NAND strings is respectively coupled to the first bias node; and

wherein the second end of each of the first group of the NAND strings is respectively coupled to the second bias node, and the second end of each of the second group of the NAND strings is respectively coupled to a corresponding one of the plurality of global bit lines.

45. (Withdrawn) The integrated circuit as recited in claim 39 wherein:
pairs of NAND strings are coupled to the same global bit line, each such pair including a NAND string from each of the first and second groups of NAND strings, thereby providing for a global bit line pitch which is half that of the NAND strings.

46. (Withdrawn) The integrated circuit as recited in claim 39 wherein:
more than one physically adjacent NAND strings of the first memory block share a contact to the first or second bias nodes.

47. (Withdrawn) The integrated circuit as recited in claim 39 wherein:
each NAND string of the first memory block contacts its associated global bit line by way of a via which is shared by a corresponding NAND string of another memory block having different word lines.

48. (Withdrawn) The integrated circuit as recited in claim 39 wherein:
each NAND string of the first memory block contacts its associated global bit line by way of a via which is shared by a corresponding NAND string of another memory block disposed on another memory plane.

49. (Withdrawn) The integrated circuit as recited in claim 39 wherein:
each of the first group of NAND strings of the first memory block contacts its associated global bit line by way of a via which is shared by a NAND string of another memory block on the same memory plane as the first memory block.

50. (Withdrawn) The integrated circuit as recited in claim 39 wherein:
the memory cell devices comprise transistors having a charge storage dielectric.

51. (Withdrawn) The integrated circuit as recited in claim 39 wherein:
the memory cell devices comprise transistors having a respective threshold voltage which is modifiable post-manufacture.

52. (Withdrawn) The integrated circuit as recited in claim 39 wherein:
the first and second plurality of block select devices of a given NAND string are structurally identical to the memory cell transistors of the given NAND string.

53. (Withdrawn) The integrated circuit as recited in claim 39 wherein:
the memory cell transistors of a given NAND string have a depletion mode threshold voltage for at least one of two data states.

54. (Withdrawn) The integrated circuit as recited in claim 39 embodied in computer readable descriptive form suitable for use in design, test or fabrication of said integrated circuit.

55-60. (Canceled)

EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. § 1.130, 1.131, or 1.132 or any other evidence entered by the examiner and relied upon by appellant in the appeal.

RELATED APPEALS APPENDIX

There are no decisions rendered by a court or the Board in any proceeding identified above in the Related Appeals and Interferences section.